Millimeter-Wave InP Lateral Transferred-Electron Oscillators

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Abstract—**We have investigated a lateral InP transferred-electron device (TED) designed with a high-resistivity notch adjacent to the cathode contact and demonstrated its application to millimeter-wave monolithic integrated circuits (MMIC's). At 29.9 GHz, a CW power output of 29.1 mW with a conversion efficiency of 6.7 percent has been obtained from cavity-tuned discrete devices. This result represents the highest power output and efficiency of a lateral TED in this frequency range. The lateral devices also had a CW power output of 0.4 mW at 98.5 GHz and 0.9 mW at 75.2 GHz. In addition, a monolithic oscillator incorporating the lateral TED has been demonstrated at 79.9 GHz. Experimental and theoretical results are presented which further the understanding of the lateral device operation.**

I. INTRODUCTION

THE MATERIAL properties of InP are excellent for transferred-electron device (TED) operation in the millimeter-wave region. Compared to GaAs, InP has a higher and less temperature sensitive peak-to-valley velocity ratio, a higher thermal conductivity, a lower electron diffusion constant, and faster central valley electron dynamics [1]. The utilization of these material properties has led to the development of high-efficiency mm-wave oscillators and low-noise broad-band mm-wave amplifiers [2]–[4]. Typical device structures have the current flow perpendicular to the wafer surface and employ n^+ substrates or thick n^+ layers grown on semi-insulating substrates. The use of n^+ substrates or thick n^+ layers makes monolithic integration with other devices difficult to achieve. This work focuses on the development of a lateral TED which is more suitable for integration in mm-wave monolithic circuits.

We have previously reported on *X*-band (8.2–12.4 GHz) lateral InP transferred-electron oscillators which had a localized high-resistivity region adjacent to the cathode contact [5], [6]. The high-resistivity region, referred to as a notch, partially extended into the active layer and was formed by selective implantation damage. This device design was implemented to create a localized high electric field region, which would produce a laterally uniform, well-defined space-charge nucleation site. Computer simulations described in this paper confirm this conceptual model of device operation. The notched devices demonstrated significantly superior microwave performance compared with devices without a notch. At *X*-band the notched devices operated with dc-to-RF conversion efficiencies of up to 9.5 percent while the devices without a notch operated with efficiencies of less than 1 percent.

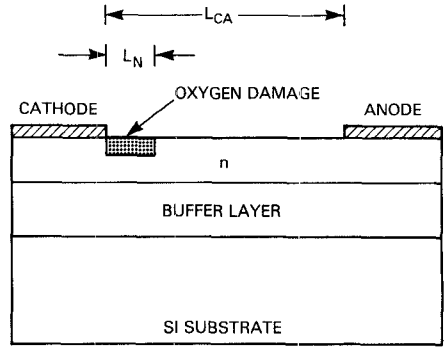

Fig. 1. Discrete device cross section. The notch length, L_N, was 0.4 μm. Devices were fabricated with lengths L_{CA} of 1.5, 2.7, 3.5, 4.5, 8.0, and 12.0 μm.

In this paper, we report the mm-wave performance of the lateral TED and its demonstration in a mm-wave monolithic circuit. From cavity-tuned discrete devices a power output of 29.1 mW with a dc-to-RF conversion efficiency of 6.7 percent has been demonstrated at 29.9 GHz. At higher frequencies, CW power outputs of 0.9 mW and 0.4 mW have been obtained at 75.2 GHz and 98.5 GHz, respectively. Initial work on an 80 GHz monolithic oscillator incorporating the lateral TED will be described. Experimental and theoretical results are also presented which further the understanding of lateral device operation.

II. DISCRETE DEVICE DESIGN AND FABRICATION

The device cross section and the discrete device layout are shown in Figs. 1 and 2, respectively. The devices were fabricated with a notch length of 0.4 μm and cathode-to-anode spacings of 1.5, 2.7, 3.5, 4.5, 8.0, and 12.0 μm. The device width was 100 μm. The material used was n-type vapor phase epitaxial InP grown with an unintentionally doped buffer layer on an Fe-doped semi-insulating substrate. For the discrete devices the active layer carrier

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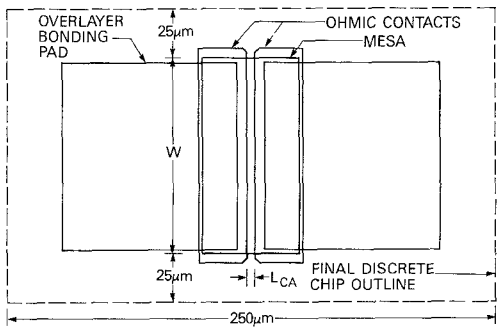

Fig. 2. Discrete device layout. The device width, W, was 100 μm for the discrete devices and 200 μm for the devices incorporated in the monolithic oscillator.

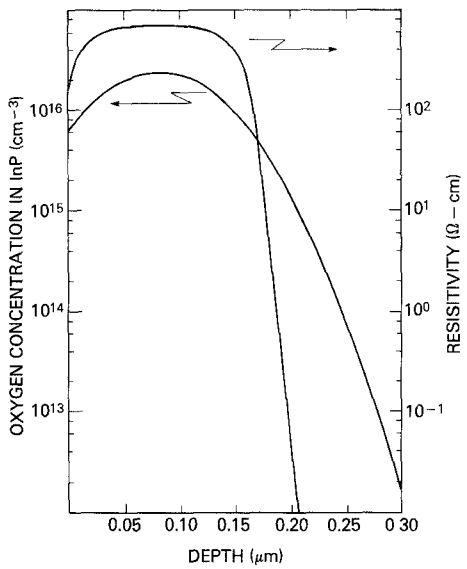

Fig. 3. Calculated oxygen concentration in InP versus depth and the resistivity of the oxygen-implanted InP versus depth.

concentration was 3×10^{16} cm^{-3} with a thickness of 0.9 μm. This carrier concentration and thickness were chosen to exceed the *nl* and *nd* products of 10^{13} cm^{-2} and 10^{12} cm^{-2}, respectively [7].

To begin device fabrication, the cathode and anode metallization patterns were defined in photoresist and AuGe/Au (1000/1000 Å) was slant evaporated at an angle of approximately 25° with respect to the wafer normal. Using the metallization as a mask, oxygen was implanted at an energy of 50 keV and a fluence of 3.0×10^{11} cm^{-2} into the regions that were left exposed after the slant evaporation. The resistivity of the oxygen-implanted region is thermally stable to 450°C [8]. Using the implantation parameters for oxygen in InP [9], the oxygen concentration as a function of depth in the notch region can be calculated and is shown in Fig. 3. From the calculated oxygen concentration and the resistivity of oxygen-implanted InP as a function of fluence [8], the resistivity of the notch region as a function of depth can be determined and is shown in Fig. 3. The notch depth is estimated to be 0.2 μm. This is the depth at which the resistivity of the notch region equals the resistivity of the active channel.

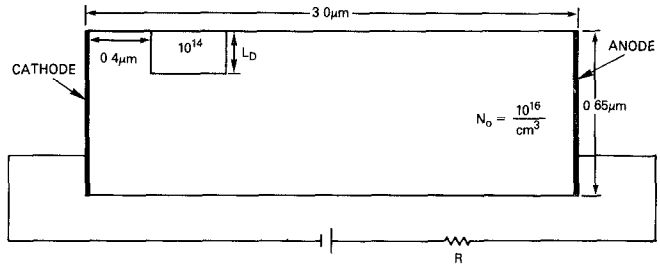

Fig. 4. Simulated device structure and circuit. The notch depth, L_D, is 22, 44, or 66 percent of the channel thickness. The notch region was simulated with a donor doping level of 1×10^{14} cm^{-3}. The resistor, R, was equal to the low field resistance of the device.

After the oxygen implantation the cathode and anode patterns were defined by lift-off. The sample was then alloyed on a hot plate at 420°C for 60 seconds in a N_2/H_2 (90/10 percent) ambient. The contact resistance was measured to be 0.6 Ω·mm by the transmission line method [10]. Device mesas were etched in a (1000:80:6:1 H_2O:HBr:KBr:Br_2) solution. The device bonding pads shown in Fig. 2 were formed by the lift-off of Cr/Au (50/4000 Å). The wafers were then lapped to 100 μm and the individual devices were scribed and separated.

Two-dimensional computer simulations on a related device structure have been performed. The numerical simulation used an algorithm that solves Poisson's equation, the equation of continuity, and the semiconductor drift and diffusion equation [11]. The simulated device structure is shown in Fig. 4. The contacts were at the ends of the device, and for the information presented here the notch depth, L_D, was 22, 44, or 66 percent of the channel thickness. The notch region was simulated with a donor doping level of 1×10^{14} cm^{-3} and the simulated notch length was 0.5 μm. The device was modeled in the resistive circuit shown in Fig. 4, with the resistor, R, equal to the low field resistance of the device. In these simulations, a dipole domain was observed to nucleate underneath the notch, to grow and propagate toward the anode, to be collected at the anode, and to recycle. This sequence of nucleation, propagation, and collection is pictured for a 22 percent notch in Fig. 5. In this figure, the plotted carrier density is shown for a line extending along the bottom of the device. In the simulation, the frequency of oscillation was approximately 40 GHz, which corresponds to an effective domain velocity of 1.0×10^7 cm/s for the transit length of 2.6 μm. While these two-dimensional simulations in a resistive circuit point to the existence of a dipole domain transit time oscillation, the mode of operation in a reactive circuit would likely result in transit time hybrid-mode oscillations such as delayed or quenched domain transit time oscillations [12]. Fig. 6 shows the electric potential in the device corresponding to the time sequence of Fig. 5. It is observed that the electric field, which is the slope of the potential function, is high in the notch region during the nucleation phase but is not fixed at a high level during domain propagation and collection. A device with a cathode field fixed at a high level has been shown to result in low-efficiency operation [13]. An important design param-

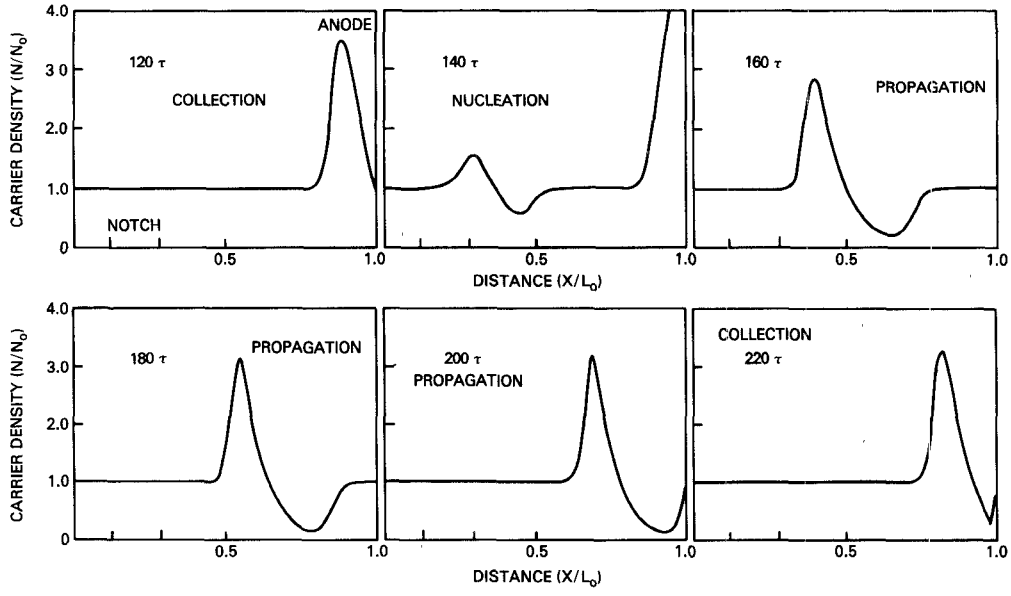

Fig. 5. Carrier density versus distance for different time intervals. The carrier concentration is shown for a line extending along the bottom of the device. $\tau = 2.25 \times 10^{-13}$ s, $L_0 = 3.0$ μm, and $N_0 = 1 \times 10^{16}$ cm^{-3}. A dipole domain nucleates underneath the notch, grows and propagates toward the anode, collects at the anode, and recycles.

eter is the percentage of channel thickness that the notch occupies. The computer simulations did not identify an optimum notch depth, but did point out that notch depths greater than 22 percent resulted in lower amplitude current oscillations. In previous experimental studies [5], an optimum notch depth was found to exist in the range of 15–35 percent of the channel thickness.

III. Discrete Device DC Characteristics and MM-Wave Performance

For discrete device characterization, devices were wire-bonded into diode packages and inserted into a tunable waveguide cavity. The equipment test setup consists of standard mm-wave measurement equipment and is shown in Fig. 7. CW operation is possible for the values of carrier concentration and thickness chosen. The $I-V$ asymmetry of a device with a 3.5 μm cathode-to-anode spacing is shown in Fig. 8. The $I-V$ curves under normal and reverse bias are similar until current saturation is reached. For the normal bias condition, the current drops back at applied voltages above the threshold voltage and the current level in the negative differential resistance region depends on circuit tuning. The $I-V$ characteristic for the device under normal bias is obtained with the device tuned for maximum power output. Under reverse bias current drop-back is not observed. Also, devices under reverse bias exhibit very poor oscillation characteristics with an ill-defined spectrum and very low efficiency. These poor operating characteristics under reverse bias are consistent with a high electric field at the positive terminal due to the notch that would prohibit efficient domain nucleation and extinction.

The $I-V$ curves of devices with cathode-to-anode spacings of 2.7 μm fabricated with and without a notch are shown in Fig. 9. The $I-V$ curves for these devices are similar until saturation current levels are reached. The

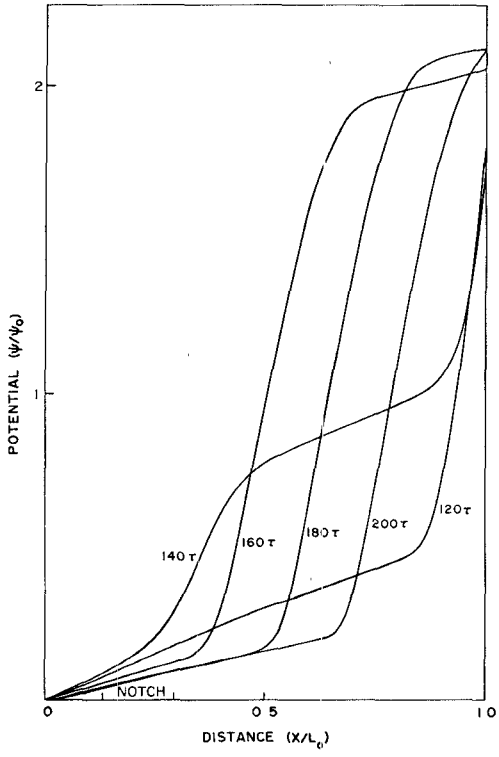

Fig. 6. Electric potential in the device at time intervals corresponding to Fig. 5. $\tau = 2.25 \times 10^{-13}$ s, $L_0 = 3.0$ μm, and $\psi_0 = 2.9$ V. The electric field corresponds to the slope of the potential function. The propagating high electric field regions are due to propagating dipole domains.

device without the notch does not exhibit current drop-back above threshold, has a much lower burnout voltage, and has poor oscillation characteristics. The poor oscillation characteristics are consistent with a lack of a well-defined space-charge nucleation site. The notched device demonstrated a CW power output of 29.1 mW with a dc-to-RF conversion efficiency of 6.7 percent at a frequency of 29.9

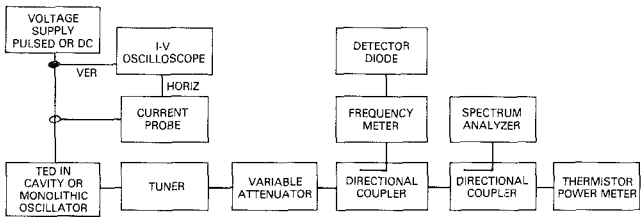

Fig. 7. Test equipment setup using standard measurement equipment.

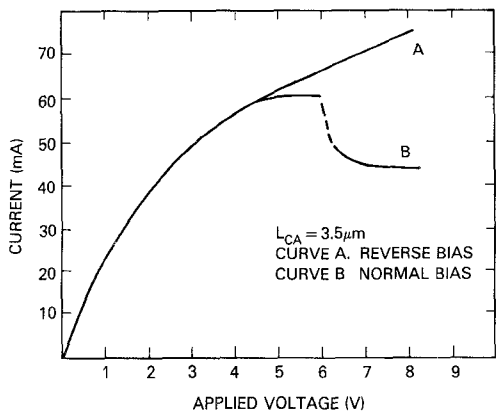

Fig. 8. $I-V$ characteristics for a 3.5-μm-long device under normal bias and reverse bias. Current drop-back is only observed under normal bias conditions.

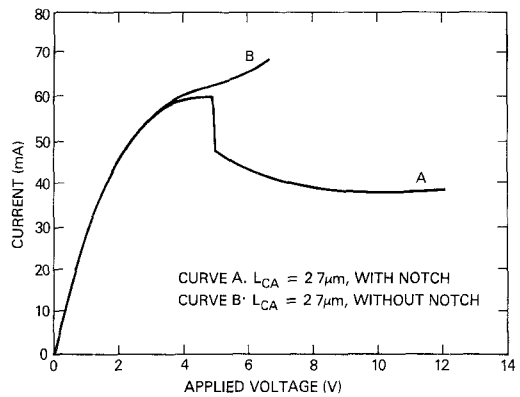

Fig. 9. $I-V$ characteristics with and without notch for a 2.7-μm-long device. The device without the notch does not exhibit current drop-back above threshold, has a much lower burnout voltage, and has poor oscillation characteristics.

GHz. This high efficiency in this frequency range is a factor of 10 greater than the efficiency achieved by InP devices fabricated without a notch and a factor of 5 greater than that reported for GaAs lateral TED's [14]. This result represents a significant advance toward achieving the efficiency of 13 percent presently obtained with current-limiting InP mesa-structure TED's [15]. Devices with a cathode-to-anode spacing of 1.5 μm have been tested at W-band (75–110 GHz). A CW power output of 0.4 mW with an efficiency of 0.2 percent at 98.5 GHz and a power output of 0.9 mW with an efficiency of 0.4 percent at 75.2 GHz have been obtained. This is believed to be the highest reported oscillation frequency obtained from a lateral TED.

The dc-to-RF conversion efficiency as a function of device cathode-to-anode spacing has been measured in a

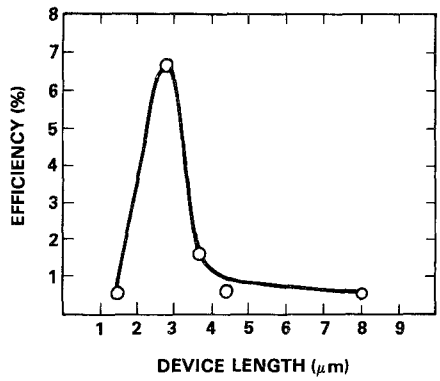

Fig. 10. dc-to RF conversion efficiency versus device length at Ka-band. A strong length dependence is displayed with maximum efficiency for a length of 2.7 μm.

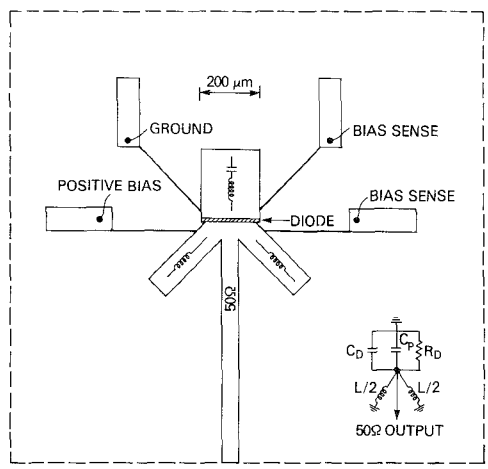

Fig. 11. Monolithic oscillator layout with an equivalent circuit shown in the inset. C_D is the device capacitance, C_p is the parasitic capacitance, R_D is the device negative resistance, and L is the shunt inductance provided by the two open-circuited stubs below the device. The open-circuited stub above the device is an RF short circuit at the oscillation frequency.

tunable waveguide cavity designed for Ka-band (26.5–40 GHz) operation. As shown in Fig. 10, the efficiency of the lateral notched TED's depends strongly on device length; therefore, the device length is regarded as a key design parameter. A maximum in efficiency is observed for a length of 2.7 μm. The maximum in efficiency is attributed to the matching of the transit length of the device to the frequency of the circuit. The modeling of other investigators has suggested a transit time insensitive mode of operation for this device structure [16]. In the transit time insensitive mode, the device length could vary over a wide range without power level degradation. The evidence presented here appears to be inconsistent with a transit time insensitive mode of operation.

IV. Monolithic Oscillator

The monolithic oscillator layout is shown in Fig. 11. The cross section of the device used in the monolithic oscillator is similar to that of the discrete devices shown in Fig. 1. For the monolithic oscillator the active layer carrier concentration was 5×10^{16} cm^{-3} and the device width was 200

μm. The width of 200 μm was chosen for optimum negative resistance magnitude, and as a reasonable compromise between device thickness and resonator width. The devices used in the monolithic oscillator were fabricated with an n^+ anode. The n^+ anode was used to achieve low anode fields and a higher device burnout voltage [17]. The n^+ anode was formed by selective Si implantation at energies of 30, 100, and 250 keV with fluences of 0.86, 2.2, and 6.6×10^{13} cm^{-2}, respectively. To activate the n^+ implant the sample was proximity annealed at 725°C for 15 min in a N_2/H_2 (90/10 percent) ambient [18]. This procedure produced a layer about 0.3 μm thick with a carrier concentration of 1×10^{18} cm^{-3} and a room-temperature Hall mobility of 1900 cm^2/V-s. The distance from the cathode to the n^+ implanted region was 2.0 μm. The distance from the edge of the n^+ implanted region to the anode metallization was 1.5 μm. The ohmic contacts and the notched region were formed as previously described for the discrete devices. The circuit metallization shown in Fig. 11 was formed by the lift-off of Cr/Au (50/6000 Å). After the circuit metallization was lifted, the wafer was lapped to a thickness of 75 μm. One μm of Al was evaporated on the backside of the wafer to form the microstrip ground plane. The final chip size of the monolithic oscillators was 1.5 mm by 1.6 mm.

The monolithic oscillator was designed by assuming a diode equivalent circuit of an active negative resistance, R_D, in parallel with an active capacitance, C_D, as shown in the inset of Fig. 11. The parasitic capacitance, C_p, is predominantly the capacitance between the surface metallization on opposite sides of the diode and was calculated to be 0.12 pF. The diode area was chosen to make R_D approximately -50 Ω, and the active diode capacitance used was approximately 0.1 pF [19].

The distributed circuit of Fig. 11 was designed so that the magnitude of the device negative resistance would equal the load resistance and that the reactance of the diode and parasitic capacitance would equal the reactance of the shunt inductance. The designs were for a substrate thickness of 75 μm, an InP dielectric constant of 12.55, and a frequency of 75 GHz. The RF short circuit on one side of the InP device was provided by a quarter-wavelength open-circuited stub whose characteristic impedance was 24 Ω and whose dissipation loss was 0.27 dB per wavelength. The lengths of this line and of all the other open-circuited lines were corrected for end-fringing capacitance. The shunt inductance at the other side of the InP device was provided by the two identical open-circuited stubs, having a characteristic impedance of 43 Ω and loss of 0.31 dB per wavelength. Their total equivalent inductance was selected to resonate at the desired operating frequency with the 0.22 pF of total capacitance estimated for the sum of the active diode capacitance and the parasitic capacitance. The distributed circuit was made physically symmetrical to help ensure that the RF field pattern in the diode and in the RF grounding stub remained in the dominant quasi-TEM configuration, rather than in a laterally asymmetrical mode. The transmission line circuitry was computer optimized with losses included in the analysis. The dc bias circuitry used quarter-wavelength transmission lines of high (120 Ω) and low (42 Ω) characteristic impedance. Physical symmetry was maintained by using bias connections on both sides of the circuit.

To evaluate the monolithic oscillator, the 1.5 mm by 1.6 mm chip was mounted onto a special test fixture. The 50 Ω microstrip output line was connected to the inner conductor of a miniature coaxial line which then transitioned to *W*-band waveguide [20]. Due to high current levels, the device was tested with 1 μs pulses at 1 percent duty cycle to prevent thermal burnout. The threshold current level was 350 mA and the operating current was 245 mA. The threshold voltage and bias voltage, both corrected for a bias circuit resistance of 8 Ω, were 4 V and 11 V, respectively. Without external tuning, the circuit oscillated at 79.9 GHz with a pulsed power output of 0.1 mW. A waveguide tuner was used, but no more power could be obtained with external tuning. Therefore the circuit has produced approximately the correct frequency and load resistance for the diode. Experimental optimization of the device length and doping level and of the value of the load resistance is expected to result in increased power output.

V. Summary

The highest CW power output and efficiency of a lateral TED have been obtained at 30 GHz and oscillations up to 98.5 GHz have been observed. A monolithic oscillator incorporating a lateral TED has been demonstrated at 79.9 GHz. Experimental and theoretical results which enhance the understanding of the lateral TED operation have been presented. These results provide incentive for further work on lateral TED's for monolithic oscillators at 30 GHz and above.

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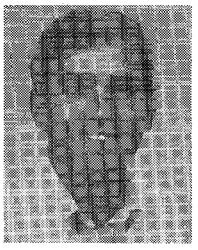

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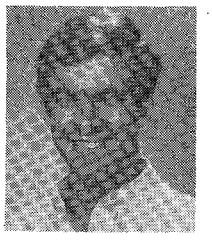

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